Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. EA**
2. **I0**
3. **I1**
4. **I2**
5. **I3**
6. **I4**
7. **I5**
8. **I6**
9. **I7**
10. **GND**
11. **N. O7**
12. **N. O6**
13. **N. O5**
14. **N. O4**
15. **N. O3**
16. **N. O2**
17. **N. O1**
18. **N. O0**
19. **N. EB**
20. **VCC**

**.090”**

**17**

**16**

**15**

**14**

**2 1 20 19 18**

**3**

**4**

**5**

**6**

**7**

**8**

**9 10 11 12 13**

**.092”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: Isolated**

**Mask Ref: HCT00T**

**APPROVED BY: DK DIE SIZE .090” X .092” DATE: 10/13/21**

**MFG: SUPERTEX THICKNESS .020” P/N: 54HCT540**

**DG 10.1.2**

#### Rev B, 7/1